In The Specification:

Please replace the paragraph beginning at line 7 of page. 6 as follows:

A3

--According to the embodiment of this invention, each coprocessor has a fixed function under a normal operating mode. In other words, each coprocessor will access or retrieve a fixed-length words from the memory according to the value in the coprocessor number field **[~~and/or~~]or** the coprocessor register field. Hence, data transmission quantity is controlled without the need for an additional register or the need to occupy a portion of the address mode information in the instruction. Moreover, chip area can be reduced and many instruction bits that are originally taken up by coprocessor memory access instructions for transferring length information can be freed up for other purposes.--

Please replace the paragraph beginning at line 16 of page. 6 as follows:

A4

--Fig. 1 is a diagram showing the architectural arrangement of a microprocessor and a coprocessor capable of implementing a coprocessor data access control method according to this invention. As shown in Fig. 1, the architecture principally includes a central processor unit (CPU) 100, a coprocessor 110 and a memory unit 120. The memory unit 120 includes cache memory and additional types of memories. The CPU 100 is used for executing central processing unit instructions to perform data processing, **and sends/receives control signals to/from the coprocessor 110 via the control signal line CS**. The central processing unit instructions includes the coprocessor memory access instructions. The coprocessor 110 is coupled to CPU 100 and the memory unit 120. The coprocessor 110 accesses and processes data words stored in the memory unit 120, addressed by one of addressing modes under control of the coprocessor memory access instructions executed by the CPU 100.--